JOINT INSTITUTE FOR NUCLEAR RESEARCH

Dzelepov Laboratory of Nuclear Problems

FINAL REPORT ON THE START PROGRAMME

Calibration Method for Silicon Photomultipliers Power Supply Sistem

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Abstract

Silicon Photomultipliers (SiPM) are solid-state light detectors of gain comparable to traditional Photomultiplier Tubes, which has made them attractive candidates for photon detection in particle detectors. As thousands of SiPMs are in use for particle detectors, namely in the DUNE (Deep Underground Neutrino Experiment) and TAO (Taishan Antineutrino Observatory) experiments, a reliable power supply is needed. Unipolar power supply was proposed and a multichannel power supply board with 128 channels was designed. Non-linearity of the high voltage Digital-Analog Converters used on the power supply board is minimized using different calibration methods proposed in this paper. Different numbers of calibration points as well as different interpolation algorithms used in reconstruction of intermediary points are compared based on the calibration time and accuracy.

Contents

1 Introduction

Deep Underground Neutrino Experiment (DUNE) [1] is an international experiment with a mission to answer fundamental questions that are at the forefront of astrophysical and particle physics research. The primary goal of the experiment is to measure neutrino interactions, from which oscillation probabilities can be determined for muon neutrinos and antineutrinos. This is done in two detectors: one near (ND) detector located near the neutrino beam source and one far detector located approximately 1300 km from the ND. The liquid argon time projection chamber as part of ND requires both charge and light readout. The light readout system uses Silicon Photomultipliers (SiPM) to read out light collection modules that detect UV LAr photons.

Taishan Antineutrino Observatory (TAO)[2] is a satellite experiment in the Jiangmen Underground Neutrino Observatory (JUNO). Its Central Detector consists of a spherical acrylic vessel filled with gadolinium doped Liquid Scintillator. The light readout from this scintillator is done using SiPMs for precise photon detection.

An important part of designing a light readout system, especially when operating thousands of SiPMs is ensuring a reliable power supply. However, due to the non-linearity power supply must be calibrated, otherwise, three main issues would arise.

SiPMs require a voltage source in order to function, and their output depends on its stability. Because of this, if the power supply is changed, the SiPM output will change, causing an inaccurate measurement. This could be avoided by recalibrating the detector as a whole, whenever the power supply or SiPM is changed, which is very inefficient. In addition, if a common power source is used for all SiPMs, hot shutdown would not be possible. In case of replacement of one of the SiPMs, the entire system has to be turned off. Therefore, instead of calibrating the entire detector, and using the same power source for all SiPMs, a controllable power supply should be calibrated and used to maintain the constant voltage of each SiPM.

Finally, the power supply can be designed in such a way to detect a potential current leak, by means of measuring the voltage drop between the set voltage and the measured SiPM bias voltage. However, the voltage drop could be of the same order as the non-linearity of the power supply, which is why a precise calibration is needed.

2 Experimental Method

2.1 Silicon Photomultipliers

Silicon Photomultipliers (SiPMs) are solid-state sensors which can be used for detection and quantification of low light signals. They are designed with high gain and high detection efficiency in mind in order to provide the possibility of single photon detection. As they are fast, compact, immune to the magnetic field, and most importantly, their gain is comparable to the one in traditional Photomultiplier Tubes (PMT) while using a significantly lower bias voltage, in recent years they have become one of the most popular devices for light detection in particle detectors.

SiPMs consist of arrays of Single-photon Avalanche Diodes (SPAD), based on a traditional PN junction, polarised with a reversed bias voltage that is greater than the breakdown voltage. This is also known as Avalanche Photodiode Geiger mode and is needed to ensure a self-sustaining avalanche. To stop the avalanche once the photon is registered a quenching circuit is used. The simplest passive circuit consists of just one quenching resistor connected to the APD in series, as shown on figure 1.

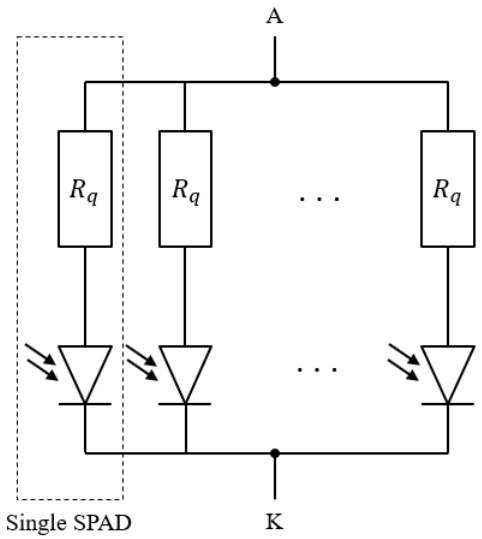

Figure 1: Silicon Photomultiplier Block Diagram

When a single photon is absorbed on one of the SPADs an avalanche process is triggered. Without a quenching circuit it would last indefinitely, however, due to the quenching resistor, bias voltage drops to the value of breakdown voltage

and the avalanche is stopped. The time between voltage dropping to breakdown voltage and its rising back to initial bias voltage is called recovery time. During this time a traditional SPAD is not able to detect any more photons, meaning it cannot be used to count photons of rate greater than the inverse of the recovery time. For this reason, many SPADs are connected in parallel, allowing simultaneous detection of more than one photon. The output of a SiPM is a superposition of outputs on all SPADs, and it can be used for either digital detection (counting) of photons or analog detection of incoming light.

A power supply for SiPM can be realized in two ways: unipolar, using just one power source on cathode side and connecting the anode to ground, or bipolar, using a high voltage source on cathode side as well as DAC on anode side. Block schemes for these two circuits are given in the figure 2.

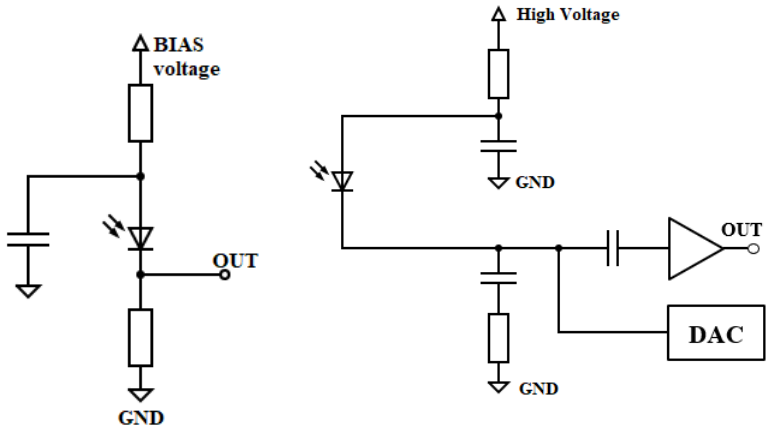

Figure 2: Unipolar (left) and Bipolar (right) Power Supply Circuit

Bipolar power supply uses a constant high voltage source and DAC chip that can be powered by a source of 5V, which is significantly less expensive than high voltage DAC required for unipolar power supply. However, unipolar supply can be Direct-Current (DC) coupled to the SiPM, and the bipolar supply needs Alternative-Current (AC) coupling. This is done using a capacitor to decouple a DC voltage from the DAC and voltage peaks that occur when a photon is detected on the SiPM. Using a capacitor for decoupling may cause problems when the peaks of the signal coming from the SiPMs are long or frequent. For this reason, unipolar power supply is proposed [3].

2.2 Power supply

In order to power a large number of silicon photomultipliers a multichannel power supply is needed. For the purposes of both TAO and DUNE experiment, the same power supply board is proposed [1]. Since the SiPMs used in these experiments are not the same, the power supply board should provide a range of different output voltages with certain precision. For instance, in the case of TAO Central Detector, required maximum voltage is 120V with the accuracy of 10mV. In order to provide scaling to thousands of channels, the power unit is to be placed in VME U6 form and the communication is realized using CAN-open protocol.

The power unit, designed by Marathon Company (MSU), consists of four Digital-Analog Converters (DAC) AD5535B chips. These are 32 channel 14-bit DAC chips with high output voltage. Each of the channels consists of a resistor string DAC and a high voltage amplifier with the nominal gain of 50V. Depending on the reference voltage on the chip the output range can be from 0V to 50V in case of reference voltage set to $V_{ref} = 1V$ and up to 200V with the reference voltage $V_{ref} = 4V$. This is needed to ensure that the board can supply different SiPMs across different experiments. The ideal DAC output voltage is given in the equation 1.

$$V_{OUT} = \frac{50 \cdot V_{ref} \cdot D}{2^{14}} \tag{1}$$

Where D is a decimal representation of the binary input code, $D \in (0, 16384)$, and reference voltage $V_{ref} \in 1, 2, 2.5, 4V$

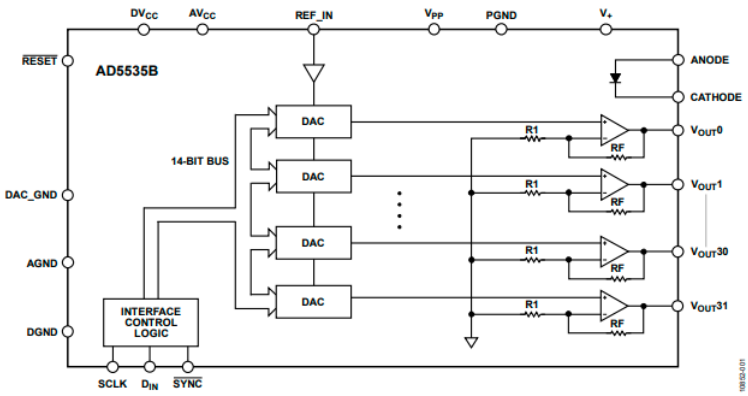

Figure 3: Functional block diagram of one AD5535B chip, from DAC AD5535B chip datasheet

In total, this board can provide 128 channels and a full range output voltage of 200V at maximum using reference voltage of 4V, as well as a full range up to

124V using the reference voltage of 2.5V, which is sufficient for the power supply needed in TAO experiment. The board is shown on figure 4, and a functional block diagram of the DAC chip is shown on figure 3.

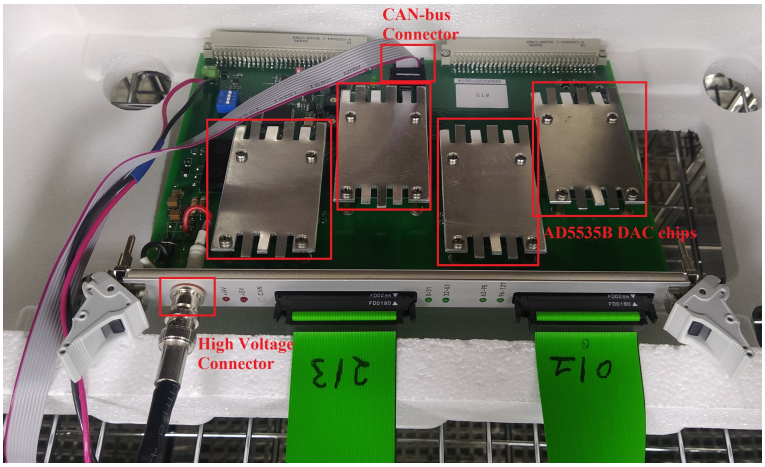

Figure 4: Power supply unit

The output for each of 128 channels is provided via two 68 pin connectors and a CAN connector is used for communication. The board is powered by two power sources, one of 5V and another high voltage one, required for the amplifier in the DAC chips.

Output voltage to a SiPM, or Keithley 2000 in the case of tests, is connected to the channel after short circuit protection, realized as a $10k\Omega$ resistor for every DAC channel. In addition to the short circuit protection, there is a voltage divider with a single channel 24 bit Analog-Digital Converter on the other end. When the ADC is properly calibrated, it can be used for the output voltage reading of the board, as well as used to measure the DAC output current via voltage drop, indicating potential current leakage or a short circuit. A functional block diagram of this connection is shown on figure 5.

In order to obtain the accurate voltage for SiPM power supply the calibration of each channel is needed. Since the 14 bit DAC is used, the total number of points that should be measured is 16 384. Calibration of the whole set of points takes about 18 hours per channel, which is not efficient. To reduce the calibration time only a small set of points should be measured. Based on these measurements, an interpolation algorithm should be applied to reconstruct the value of the remaining points, which meets the precision of 10mV per channel.

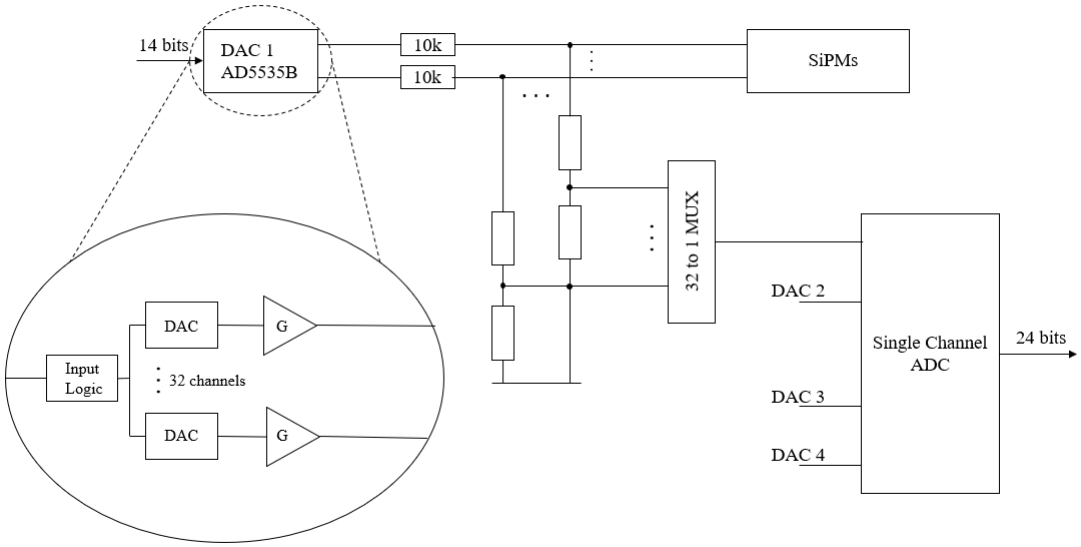

Figure 5: Functional block diagram of one DAC chip and ACD

2.3 Methods of Measurement

To calibrate one board, the measurement is performed for each of the 128 channels one at a time by scanning the input from 0 to 16 383 bits using the optimal step. The output voltage is measured with a precise multimeter and stored for use in the reconstruction of intermediary points.

Channel outputs are connected to a multiplexer via two micro coaxial cables, shown in figure 6. The multiplexer consists of a matrix of 8x16 relays and is controlled by a Raspberry Pi. The Raspberry Pi determines which channel should be read out at the multiplexer output.

The output of the multiplexer is a voltage from a single channel that is connected to Keithley 2000, a precise multimeter, to determine its actual value. The value obtained from this multimeter is sent to the PC. The entire setup is shown on the picture 6, and the setup schematic is shown on picture 7.

For the calibration purposes, external USB-CAN is used for communication between the power unit and the PC, however, in the experiment a control unit board will be placed among other power units in the VME crate.

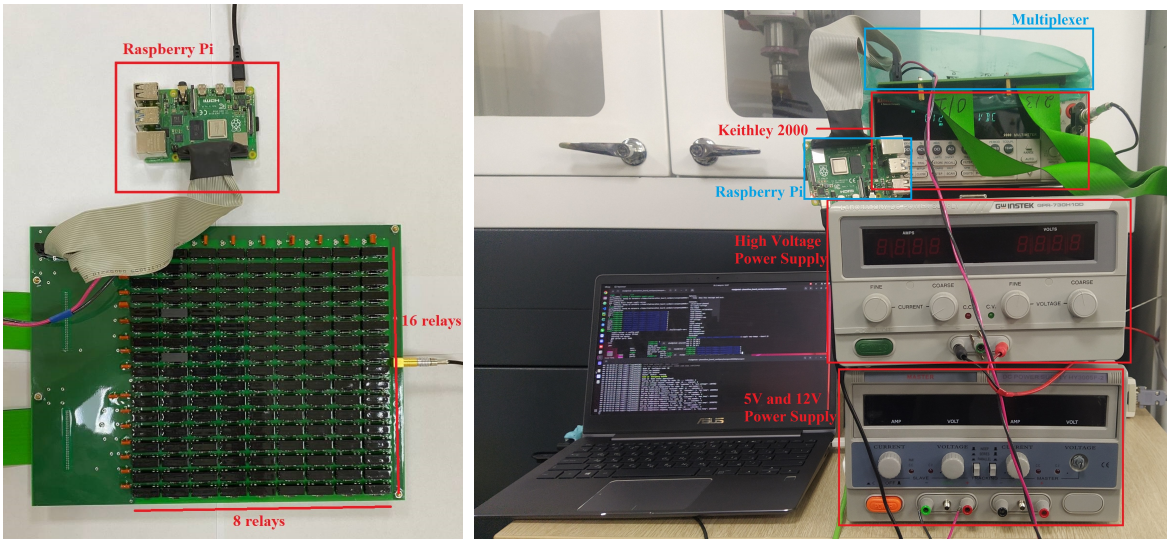

Figure 6: Multiplexer and Raspberry Pi (left) and Measurement setup (right)

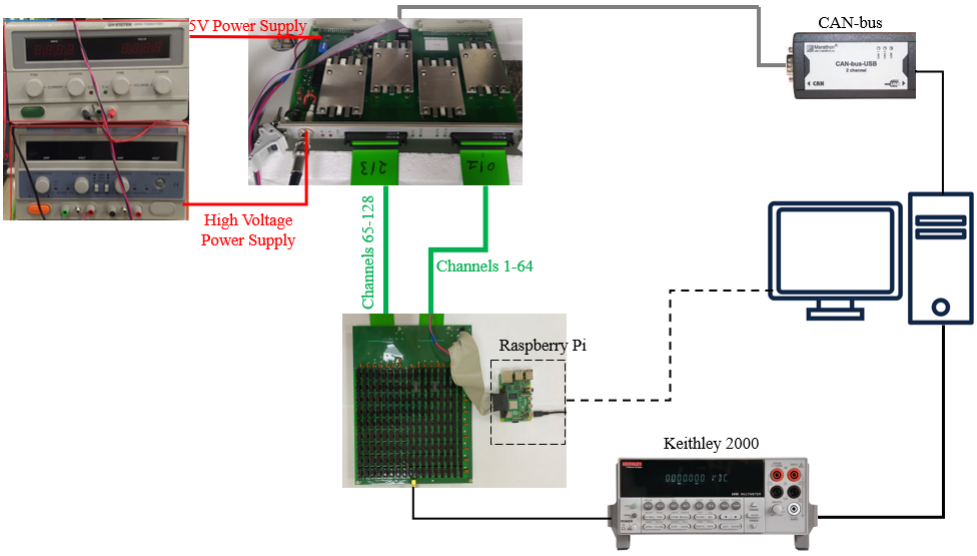

Figure 7: Measurement Setup Schematic

3 Analisys

3.1 Introduction

Digital-Analog converter (DAC) is a device that converts a digital signal from a computer to an analog voltage, typically used to power an electrical device. In this instance, the output voltage from the DAC on the power supply unit is used to supply the SiPMs.

Non-linearity parameter of a DAC can be defined as the maximum deviation of the output voltage from an ideal straight line from zero-scale to full-scale outputs. Non-linearity, expressed in Least Significant Bit (LSB), for one of DAC channels in AD5535B chip, with a maximum output voltage of 200V is shown on figure 8. The definition of LSB is given in equation 2 and in this case has a value of around $12\frac{mV}{1bit}$.

$$LSB = \frac{V_{MAX}}{2^{14}} \tag{2}$$

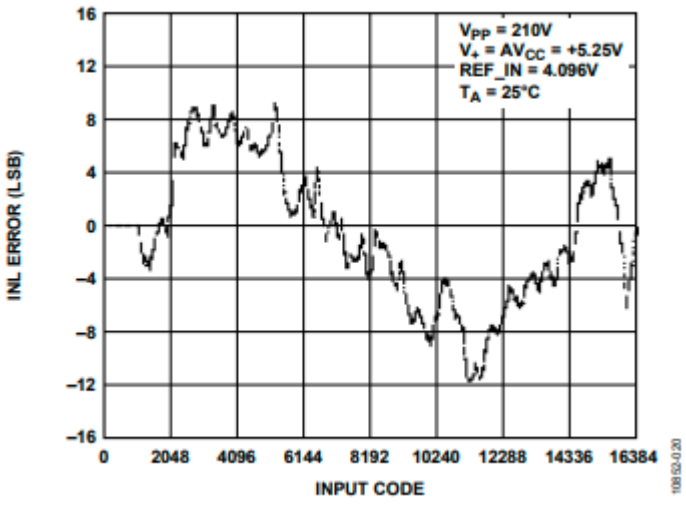

Figure 8: Non-linearity of one DAC channel with maximum output voltage of 200V, from DAC AD5535B chip datasheet

3.2 Calibration method

In order to minimize non-linearity a calibration of DAC is needed. Since one channel of DAC is 14 bits, measuring output voltage when the input signal is screened in the range from 0 to 16 384 will result in an accurate transfer function. Considering this measurement takes around 18 hours per channel and must be performed for each channel individually, acquiring an accurate transfer function for every channel is inefficient.

The reduction of the number of points and the subsequent reconstruction of the intermediate points provide a less precise transfer function, but in much less time. The reduction of the points is done by selecting the points to be measured with a step of a certain size, chosen as a compromise between the calibration time and accuracy. Then, intermediate points should be reconstructed using an appropriate interpolation algorithm.

To confirm that this method can be applied, figure 9 shows non-linearity in LSB, measured for the full set of points with the reference voltage of 4V, then, from the non-linearity graph, 64 points are chosen equidistantly and values between them are interpolated. Difference between these non-linearities is represented as a distribution in the histogram on figure 10.

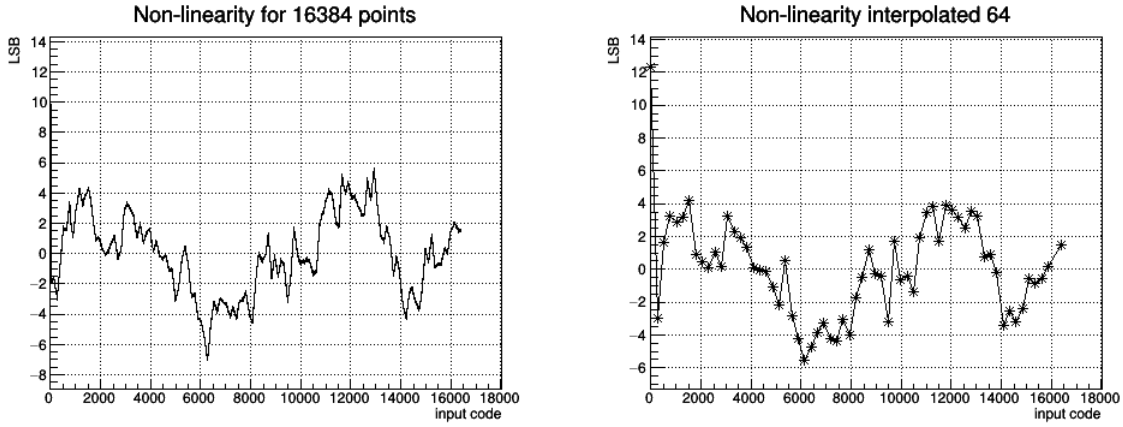

Figure 9: Non-linearity for a full set of points (left) and 64 points chosen from the non-linearity of the full set with interpolated intermediate points (right)

From figure 10 it can be concluded that the maximum difference between the real non-linearity curve and the one interpolated from a set of 64 points is around 2LSB, which is 24mV with the reference voltage of 4V. This shows that selecting a smaller set of points from the full set is sufficient for the reconstruction of the

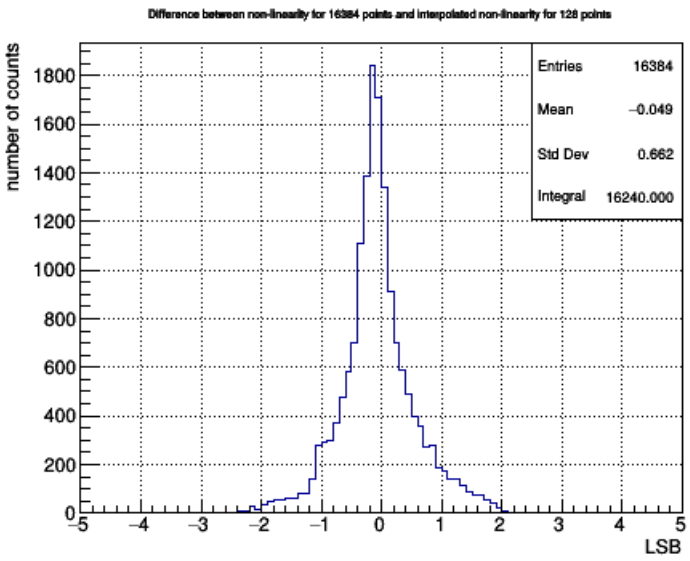

Figure 10: Difference between original non-linearity and non-linearity interpolated for 64 points

whole transfer function. In Chapter 3 Optimum number of points, different number of points are proposed in order to further decrease the standard deviation of this histogram.

To confirm that the chosen number of points as well as the chosen algorithm are appropriate for every channel on every board, a complete measurement of a larger number of channels is needed. Input voltage for DAC is screened with a certain step in the range from 0 to 16 383 and a voltage from Keithley 2000 is obtained for every first channel on five different boards.

3.3 Optimum number of points

The chosen number of points determines the time needed to measure the full range of the DAC, screening from 0 to 16383 bits. For example, if the chosen number of points is 16384, a measurement will last as long as 18h per channel, however, if that number is reduced to 256 points, the measurement of one channel is reduced to about 17 minutes, therefore, the number of points should be as low as possible. However, reducing the number of points increases the deviation of the interpolated intermediate points from the transfer function. For this reason, the optimum number of points must be chosen in such a way as to not exceed the required accuracy, which is 10mV in the case of TAO detector.

Since non-linearity curves and transfer functions for different channels have different shapes, in order for the algorithm not to favor one channel over the other, the points should be chosen equidistantly. The numbers of points chosen for testing are 32, 64, 128 and 256 and non-linearity distribution for each of the sets with linear spline interpolation, calculated for one channel is shown on figure 11.

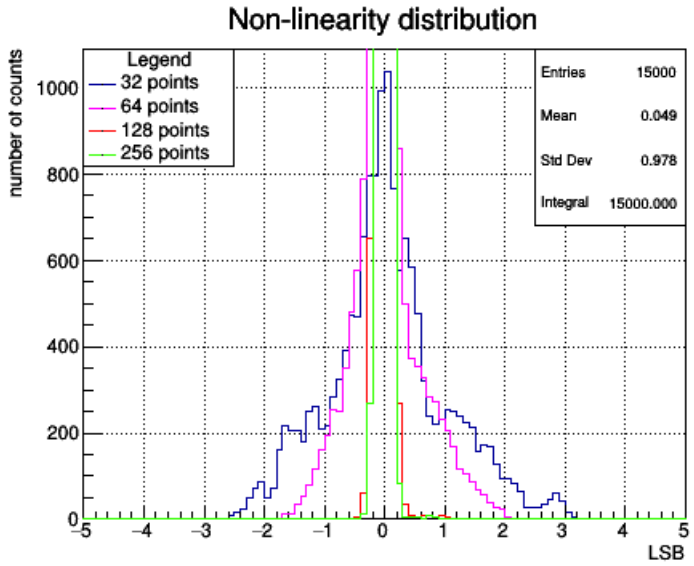

Figure 11: Non-linearity distribution for different sets of points using Linear Spline Interpolation algorithm

As shown on figure 11, for this particular channel it can be calculated that the set of 64 points has the maximum non-linearity of around 24mV for the reference voltage of 4V. However, the set of 128 points has a maximum non-linearity of around 7mV and therefore is the set with the least amount of points that meets the accuracy of 10mV. For comparison, the set of 256 points is displayed, but as there is no significant difference between the two, it is suggested that there is no need to measure additional points.

3.4 Spline Interpolation

The reconstruction of intermediate points can be executed using a uniform spline, or a piecewise polynomial algorithm. The measured points define disjointed subintervals and each one of them is fitted with an individual polynomial. For the purpose of this calibration the spline in use is either first (linear), second (quadratic) or third (cubic) degree polynomial.

Different calibration algorithms are tested on a set of 128 points and a non-linearity distribution is derived for each one. Comparison of non-linearity distributions for different spline degrees is shown in figure 12.

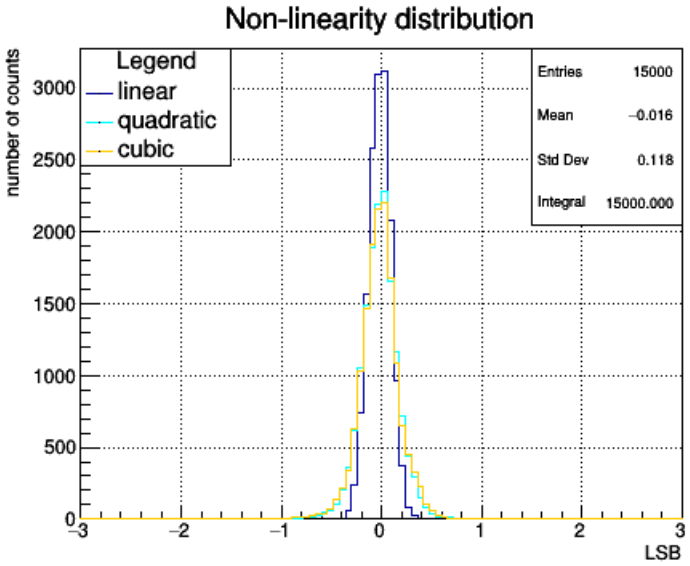

Figure 12: Non-linearity distribution for different degrees of Spline Interpolation on a set of 128 points

As shown on figure 12, linear spline algorithm in this case provides the best accuracy of the three algorithms compared, which suggests there is no need to further increase the degree of spline.

3.5 Interpolation using Fourier Transform

As an alternative to the spline interpolation algorithm, interpolation by means of zero-padding Fourier transform is performed. Modifying a function by adding an array of zeros to it, also known as zero-padding, can be done at the functions end in order to obtain a Fourier transform with more samples than the one of the original function. However, if the array of zeros is inserted in the middle of the function's Fourier transform in the frequency domain, the inverse Fourier transform of the new frequency domain sequence will result in a function of more points than the starting one. The new function will include a number of interpolated values between the old samples.

First, a linear function is fitted throughout the 128-point sample. Then, the Fourier Transform of the non-linearity, derived as a deviation of the sampled

points from the fitted line, is zero-padded with an array of 16 256 zero values and is transformed back to the time domain using Inverse Fourier Transform. This results in an interpolated non-linearity for the transfer function, and can be later used for reconstructing the transfer function.

For comparison, non-linearity distribution of transfer function using linear spline algorithm and Fourier Interpolation of non-linearity are measured for a set of 128 points and shown in figure 13. The non-linearity distribution indicates a significantly better performance using a linear spline algorithm.

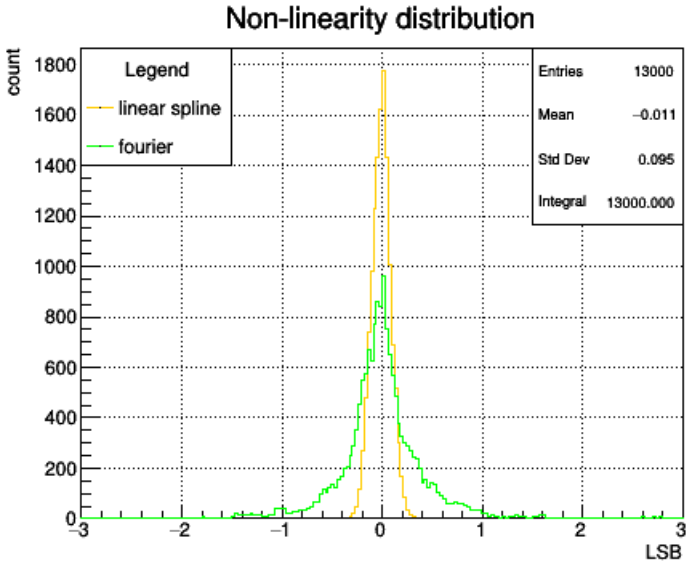

Figure 13: Non-linearity distribution for Fourier Interpolation and Spline Interpolation on a set of 128 points

4 Results

4.1 Experimental results

In order to confirm proposed solution for calibration of the power supply, different power supply boards should be measured and standard deviation of differential non-linearity compared between different calibration algorithms. Firstly, five channels on five different boards are measured in the same way as proposed in chapter 3 Calibration Method. Then, standard deviation of the non-linearity curve is calculated for sets of 32, 64, 128 and 256 points using linear spline algorithm, as well as the standard deviation for different interpolation algorithms using sets of 128 points.

Standard Deviation calculated for different sets of points, shown on the left side of figure 14 confirms that sets of 128 and 256 points are suitable for calibration across all channels. However, since measurement of 128 points is faster than the measurement of 256, there is no need to further increase the number of points.

As shown on the right side of the figure 14, a hypothesis that the linear spline algorithm has better performance than quadratic and cubic spline as well as interpolation using Fourier Transform is true across all measured channels.

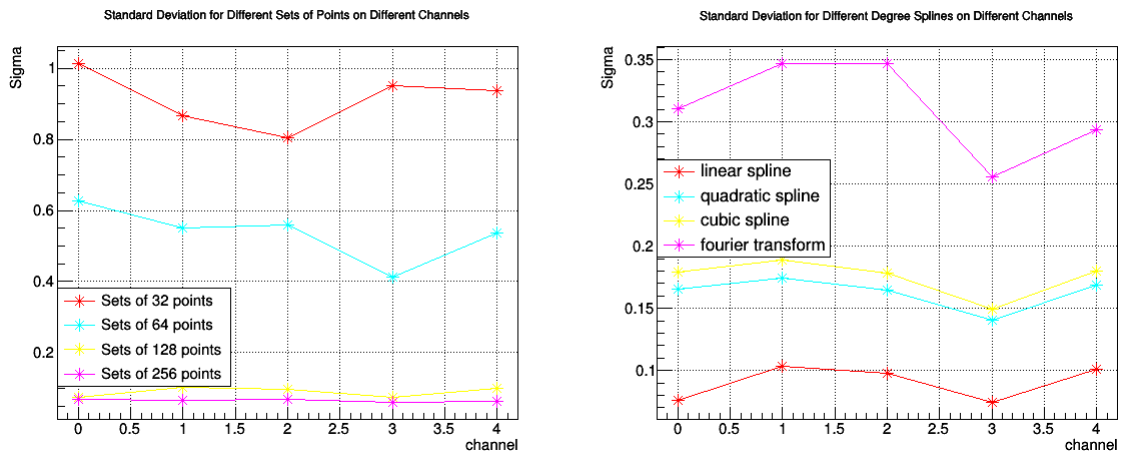

Figure 14: Standard Deviation for different sets and different splines with reference voltage of 4V

Using measurements of one of the channels, standard deviation of non-linearity using Fourier Transform and Linear Spline Interpolation for sets of even numbers of points from 64 to 256 is calculated and shown on figure 15. As expected, standard deviation decreases with the number of points and is smaller in the case of

Linear Spline Interpolation.

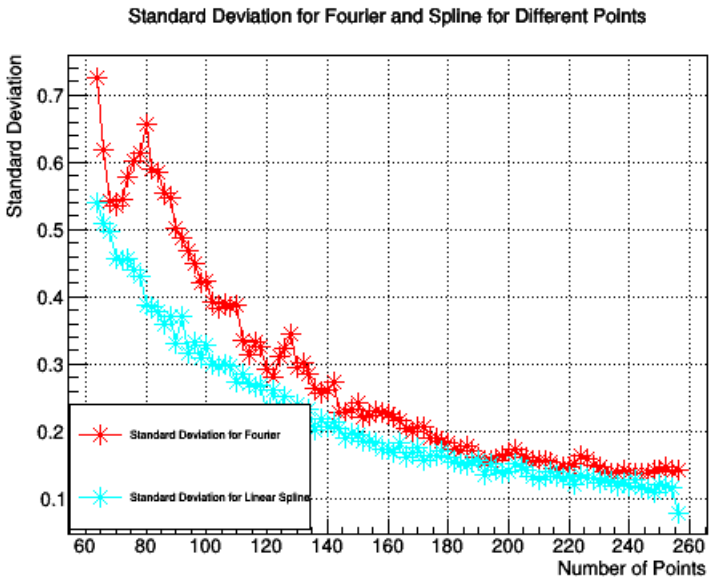

Figure 15: Standard Deviation for calibration of one channel using Fourier and Spline Interpolation for different numbers of points

4.2 Conclusion

In this paper, in order to perform a precise and efficient calibration of SiPM power supply board using high voltage DAC chips, four different sets of points are tested as well as four different interpolation algorithms. Firstly, it is determined that non-linearity measured in LSB does not depend on the reference voltage of the DAC. This ensures that calibration can be performed only for one reference voltage and then scaled accordingly to allow the use of different reference voltages.

Based on calibration of one of the channels, optimum number of points needed for the calibration is determined to be 128 and the algorithm that is the most precise is linear spline interpolation. In order to confirm this hypothesis, five different DAC channels on different boards are calibrated and the results are in line with the initial measurement.

Even though the non-linearity is not periodic, interpolation using oversampling in Fourier transform is proposed. As expected, intermediate points reconstructed in this a way deviated from the transfer function more than the ones reconstructed using the spline algorithms.

References

[1] DUNE collaboration. Deep underground neutrino experiment (dune) near detector conceptual design report. 2021.

[2] The JUNO collaboration. Tao conceptual design report. 2020.

[3] Nikolay Anfimov et al. Development of the light collection module for the liquid argon time projection chamber (lartpc). *International Conference on Instrumentation for Colliding Beam Physics Novosibirsk, Russia*, 2020.

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