Testing of self-triggered readout electronics for double-sided microstrip silicon sensors based on n-XYTER ASIC

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1. Introduction

The Compressed Baryonic Matter (CBM) experiment will be one of the major scientific pillars of the future Facility for Antiproton and Ion Research (FAIR) in Darmstadt. [1] The goal of the CBM research program is to explore the QCD phase diagram in the region of high baryon densities using high-energy nucleus-nucleus collisions. This includes the study of the equation-of-state of nuclear matter at high densities, and the search for the deconfinement and chiral phase transitions. The Silicon Tracking System (STS) is the central component of the CBM experiment.[2] It serves for track and momentum measurement of all charged particles produced at the target. A benchmark observable is the D meson (open charm), a rare probe that has to be identified via its hadronic decays $D^0 \rightarrow K^- \pi^+$ and $D^{\pm} \rightarrow K^{\mp} \pi^{\pm} \pi^{\pm}$.

This challenging task requires fast self-triggered readout, because of high multiplicity rates near 10 Mhz/cm^2. This requirement is guided by the fact that at this high rate of interactions, a good fraction of events are likely to be missed during the time of trigger decision. In the self-triggered readout system, no external event trigger is applied and all hits above a predefined threshold are recorded along with their corresponding arrival times. For this purpose STS-XYTER is being developed now, but it is not complete yet and is not well suited for spectroscopic experiments, so we use n-XYTER ASIC (Neutron-X-Y-Time-Energy Read-out Application-Specific Integrated Circuit), which firstly was developed in context of the EU-FP6 Integrated Infrastructure Initiative NMI3 in the Joint Research Activity DETNI as the common read-out solution for three different, solid converter based neutron counting area detectors. [3] It allow determining both, time of incidence as well as pulse height of the detected signals. It is only one of its kind chip, which works in self-triggered mode, has signal-to-noise ratio of 10:1, reads off signals of low amplitude of both polarities and has high reading rate.

2. n-XYTER

Because of the the statistical, non-triggerable nature of neutron data to be processed, the internal architecture of the chip is self triggered and data driven. It integrates 128 channels with low noise preamplifiers and shapers. Each channel has two different shapers with distinct time constants, one optimized for timing resolution, the other one optimized for energy (pulse height) resolution. A peak detector connected to the slower shaper allows for the application of a spectroscopic amplitude measurement. An internal time stamp generator provides the temporal reference that may be employed to identify time coincidences of signals on different detector channels and thus correlate their spatial point of origin. For testability and calibration purposes, a charge injector with adjustable pulse height was implemented. The bias settings and various other parameters can be controlled via a standard I^2C-interface.

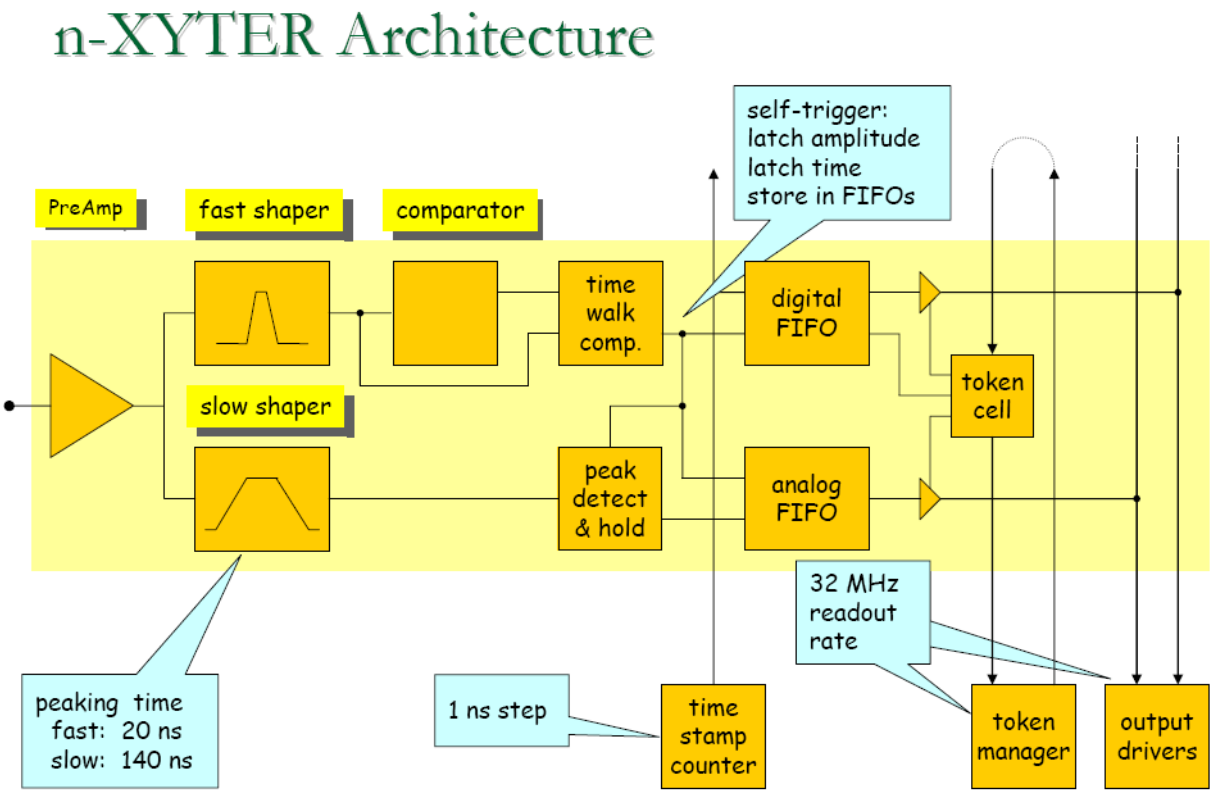

Fig. 1. n-XYTER block diagram.

So, key features of n-XYTER ASIC are:

- mixed signal chip
- process: AMS 0.35 μm CMOS
- 128 channels
- 1 test channel with analogue diagnostic output
- architecture for AC-coupling, employable for positive and negative signals
- self triggered, data driven de-randomizing, readout at 32 MHz
- digital time stamp output
- analogue peak hight output
- maximum data loss at 32 MHz average input rate over 16 μs: 4%
- analogue pile-up registry
- programmable dead time
- local threshold adjustment
- Dynamic Range: 120000 e
- Shaping time and noise performance:
  - 18 ns fast shaper at 30 pF input, 850 enc for positive signals, 1000 enc for negative signals
  - 140 ns slow shaper at 30 pF input, 600 enc
- Timing resolution ~ 2-3 ns, time stamp resolution 1 ns

Advantages of n-XYTER: high read rate, works without trigger modules.

Disadvantages of n-XYTER: high heat release (near 6 W), big noise, dependence of DC-signal levels on temperature (in n-XYTER 1.0).

2.1. Front-end

A charge sensitive preamplifier, constructed around a folded cascode circuit forms the input stage. [4] For its superior noise performance, an NMOS input transistor has been chosen. Unlike conventional readout chips, the signal path is split into two branches after the preamplifier:

- A fast CR − RC shaper, driving the timing-critical path. This branch serves to generate the time stamp and thus performs the time measurement. The time stamp may later be used to determine the time of incidence of the signal as well as to correlate signals on different channels like for example on the other coordinate in order to determine the event's locus in two dimensions. The overall gain of preamplifier and fast shaper is 47 mV/fC.
- A slow CR − (RC) 2 shaper driving the more noise-critical measurement of the deposited energy. The overall gain of preamplifier and slow shaper amounts to 24 mV/fC.

While the fast branch relies on a single-ended topology for the shaper, the slow branch is a two-stage design with a fully differential second stage. This allows the selection of the adequate signal polarity for the subsequent peak detector and hold circuit (PDH) for both polarities of the input signal. The PDH can only take positive input pulses. The precise transient response does depend upon the values of the internal registers which define the analogue operating conditions. Settings for positive and negative input charge differ in order to maximize the dynamic range within the given clipping margins. Effectively the DC operating level of the fast shaper amplifier output is shifted between 0.56 V and 1.2 V. V_{cg} is set to 1.4 V and determines the pre-amp bias current, V_{bfb} = 0.9 V controls the pre-amp feedback circuitry and V_{cm} = 1.1 V is the slow shaper's common mode output level. A schematic of the front-end is shown in Figure 2.

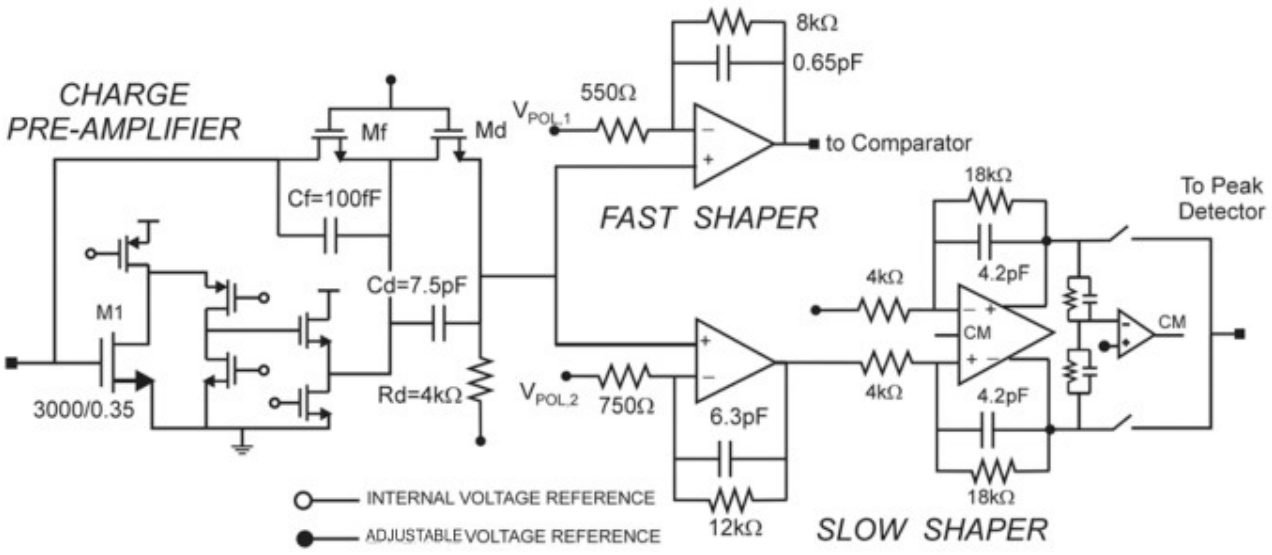

Figure 2. Schematic of the front-end, including FAST and SLOW shaper branches.

2.2. Front-end pulse shape

The front-end output signal is a semi-Gaussian pulse which can be characterized through three parameters:

- peaking time t_p (0 − 100%) or rise time t_r (10 − 90%),
- peaking voltage V_p and
- remainder R, which is the ratio between the signal voltage 25ns after the peak (V_{25+}) and V_p .

The peaking time is sometimes hard to measure since the starting point of the pulse is not well defined, so the rise time t_r (10 − 90%) is usually quoted. Figure 3 explains the various parameters.

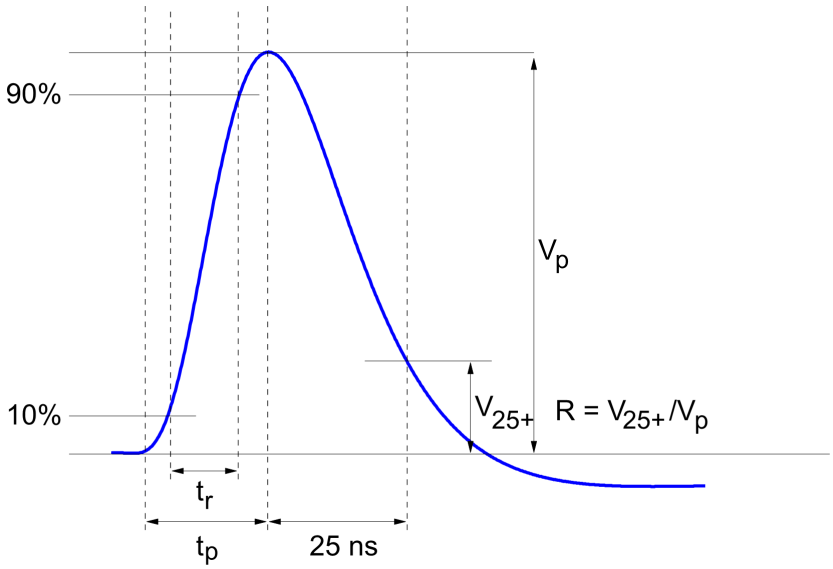

Figure 3. Semi-Gaussian pulse with the corresponding parameters characterizing shape.

2.3. Test pulse generator

An internally generated test pulse may be coupled into every channel of the ASIC when test pulse enable is selected . The amount of charge injected is controlled through register *cal*. One of four test pulse generators is activated and sends test pulses to the channels belonging to one of four groups of 32 channels. For the test pulse to be injected into any channel, the channel additionally needs to be connected to its respective coupling capacitor. This is done by means of the mask register. A mask bit 1 disconnects the channel (see figure 4).

In response to a full swing square wave at the strobe input TestPulse, the calibration circuit generates voltage steps across the capacitor coupling into the channel input. The test capacitor of C=100 fF is stimulated with a voltage step that injects the charge $Q = C \bullet \Delta V$. The step height may be programmed through I^2C register *cal* from 0 to 1.137 V.

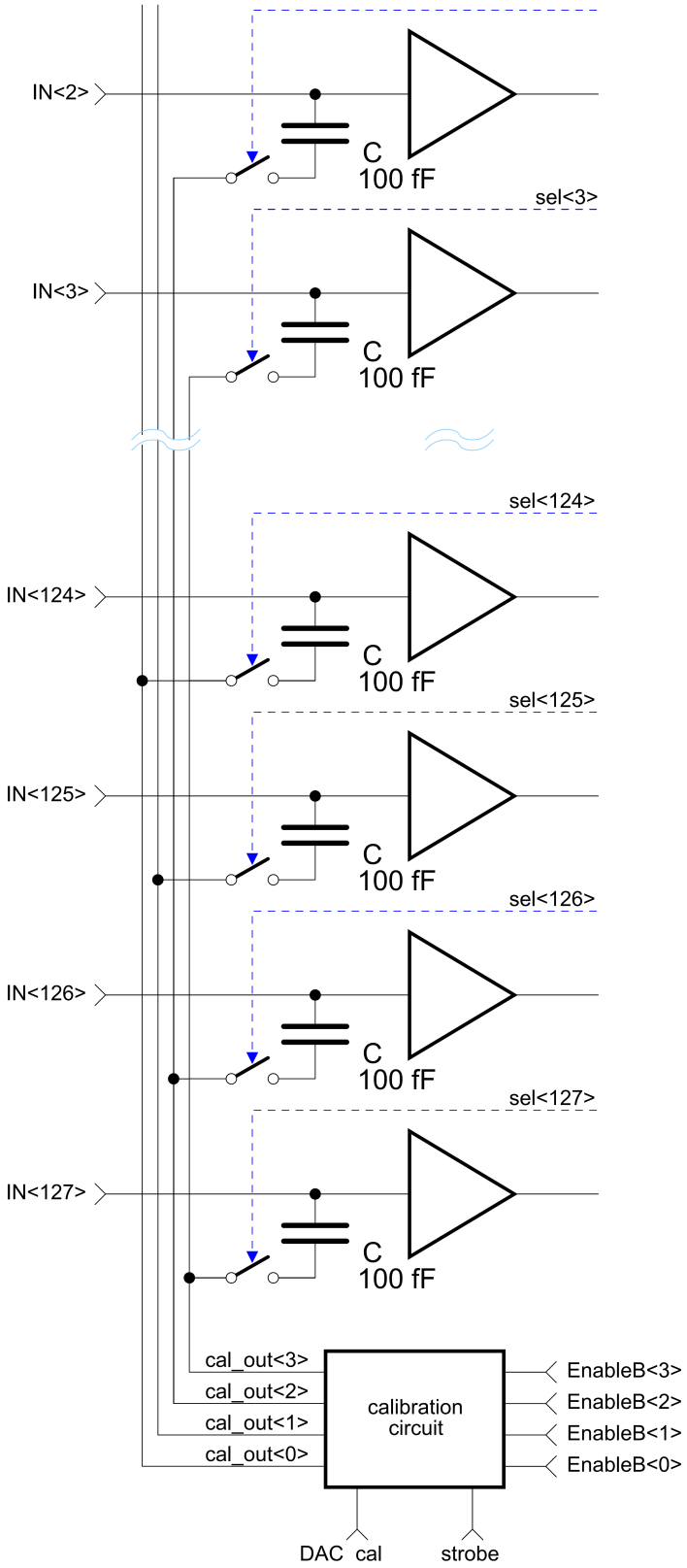

Figure 4. Block diagram of the connection between calibration circuit and channel inputs. The signals sel(127:0) are controlled through the mask registers (I^2C reg. 0 – 15), EnableB(3:0) correspond to configuration register 33 (bits 0 and 1) and the digital signal strobe corresponds to the externally applied signal TestPulse.

The corresponding injected charge at the input of the preamplifier is variable in 256 steps from 0 fC to 11.37 fC. The amount of charge injected as a function of register *cal* setting as simulated is displayed in figure 5.

Least mean square linear function fitting curve:

$$test\ charge[C] = \frac{44.41\,aC}{LSB} \cdot Reg24Value[LSB] + 182.0\,aC$$

where Reg24Value[LSB] is the value written into the *cal* register (I^2C register 24).

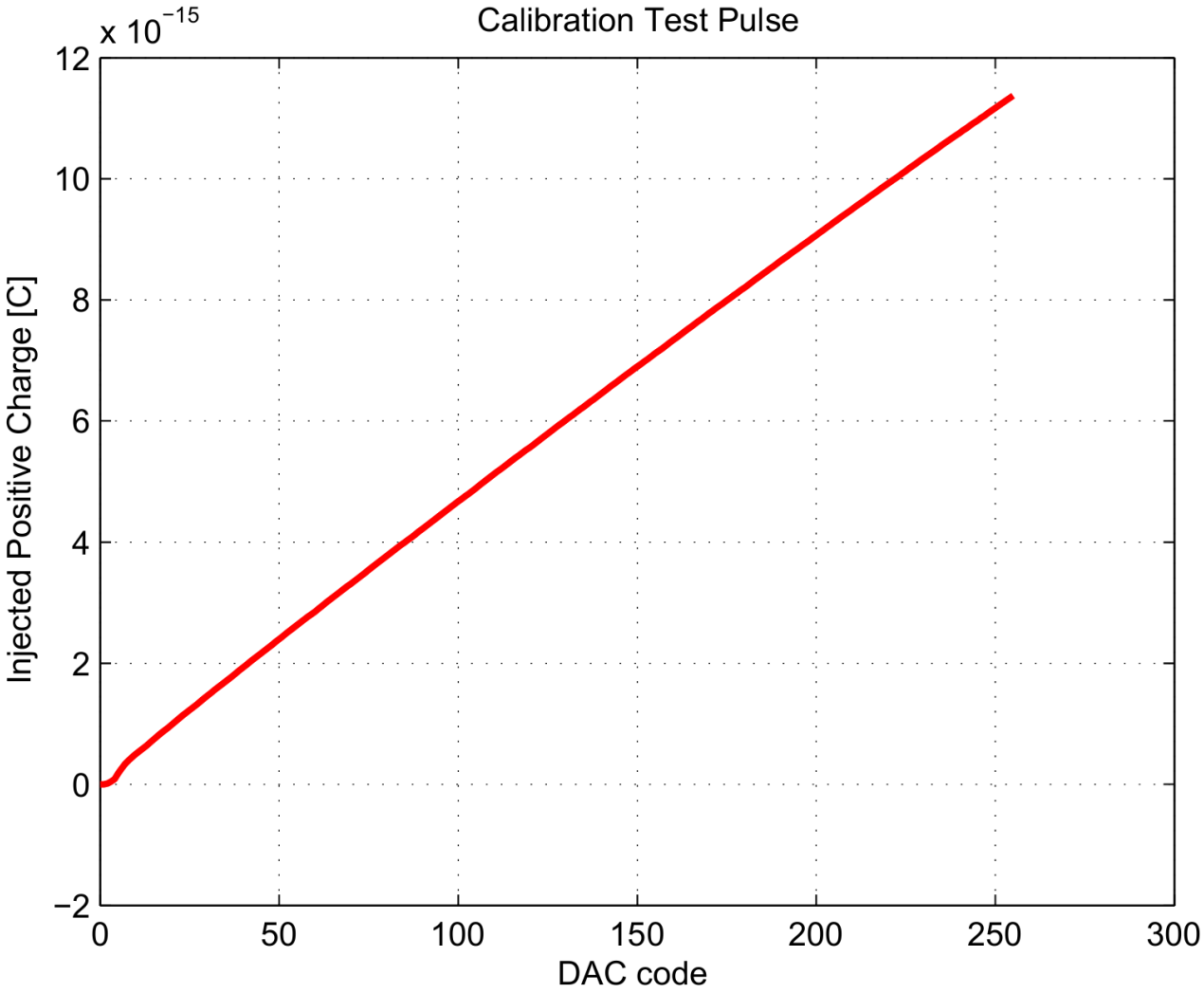

Figure 5. Injected positive charge during the calibration procedure.

3. Algorithm of calibration

With the help of *Vth* register one can set the global threshold voltage for the comparators, i.e. it defines the pulse strength that is necessary to trigger the comparator. But in every separate channel real threshold voltage differs from each other. It results from imperfection of components of ASIC and irregular distribution of gain coefficient in channels, as displayed in figure 6. [5] So for the purpose of fine adjustment of local threshold voltage Trim-DAC Shift Register is used. Additionally, this register provides a switch to individually shut-down any one or more front-end channel.

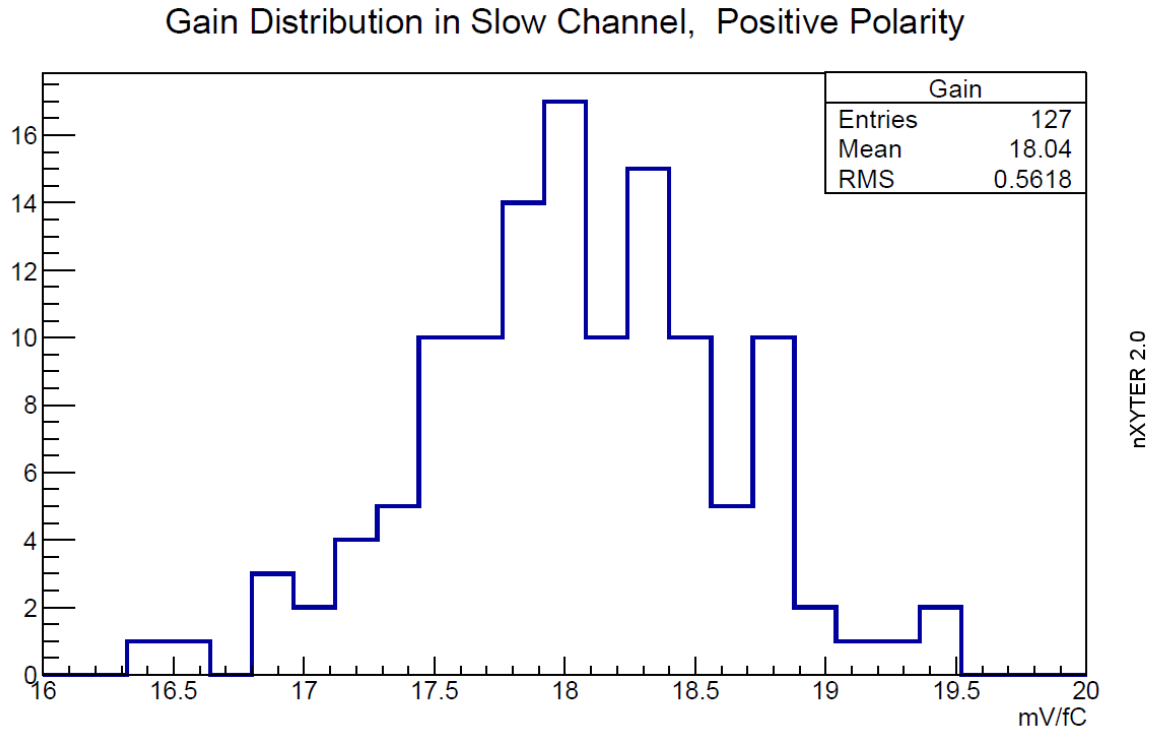

Figure 5. Distribution of gain coefficient.

For calibration I used internal test pulse generator which injects test pulses into one of four groups of channels. Frequency of these pulses is 2500 Hz, and one can calculate number of events over a period of time. One need to get a half of all events in order to reach threshold because we suppose the signal to be Gaussian. Thereto I used bisection scaling method that bisects an interval of TRIM register values and

then selects a subinterval in which an half of all events must lie for further processing.

Script was programmed on *Bash* command language with program packages *rocutil*, *dabc* and *root*. *Rocutil* permit to operate with all registers of n-XYTER rather simpler, including shift TRIM registers.

4. Test benches

There are two test benches — with n-XYTER ver. 1.0 and n-XYTER ver. 2.0 (Figures 4 and 5). The first test bench consist of n-XYTER ver. 1.0, Read-out Controller SysCore board v2.2 based on FPGA Xilinx Virtex-4 FX, colling station LAUDA Alpha RA 8 and low voltage power suppliers AKTAKOM APS-3320L and GW Instek GPS-4303.

Figure 6. Photograph of the first test bench.

In the process the second test bench was completely assembled; all cables were made. The second test bench consist of n-XYTER ver. 2.0, Read-out Controller

SysCore board v2.0 based on FPGA Xilinx Virtex-4 FX and low voltage power suppliers AKTAKOM ATH-1338 and GW Instek GPS-4303. Because of a big noise from SysCore board additional shielding of cables was necessary.

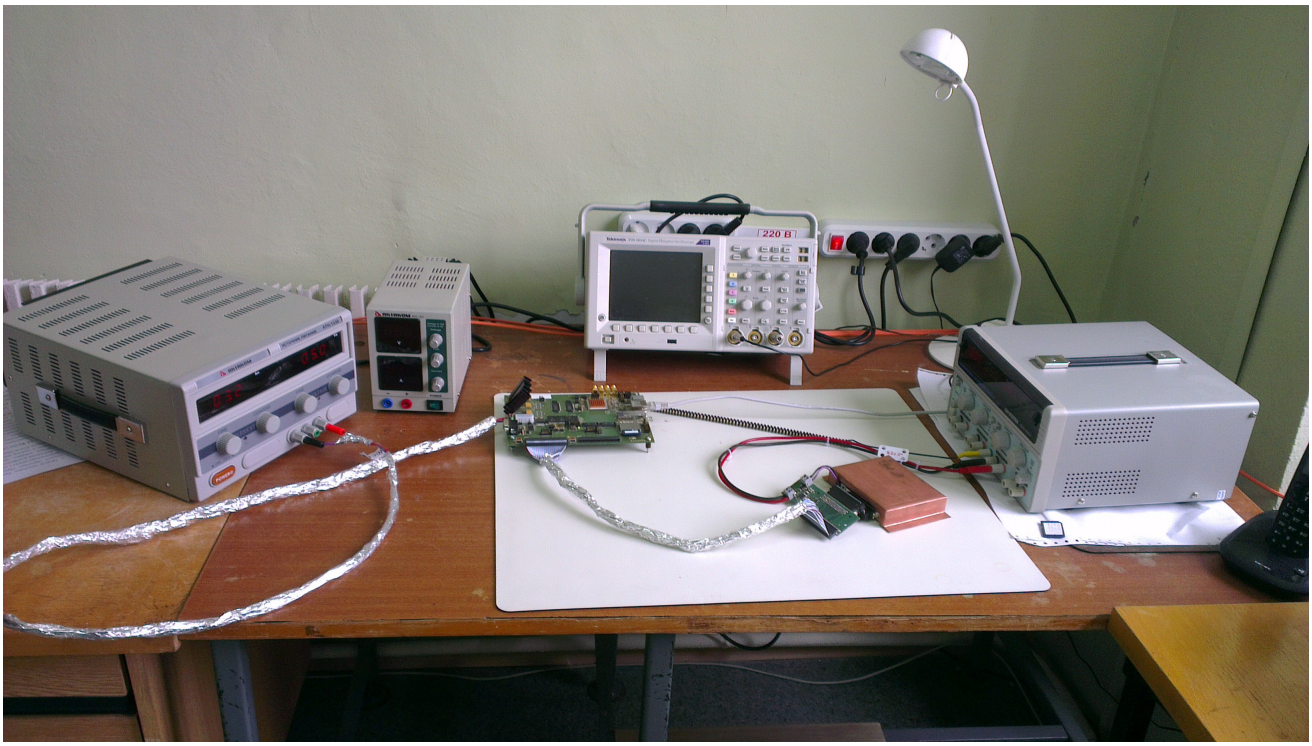

Figure 7. Photograph of the second test bench.

5. Results

Script of fine adjustment of local threshold voltages in all channels of n-XYTER was created. Algorithm was tested on n-XYTER ver. 1.0 and n-XYTER ver. 2.0. It is fully operational with n-XYTER ver. 1.0, but during a testing with n-XYTER ver. 2.0 big discreteness of TRIM register under changes of its in minimum value was exposed (as shown on figure 8), so in this case algorithm is not so effective. Figure 9 show distribution of register TRIM values over channels, which look like random distribution. Also figure 10 show histogram of values of register TRIM. Also calibration quadratic curve of *Vth* register value was built (Fig. 11).

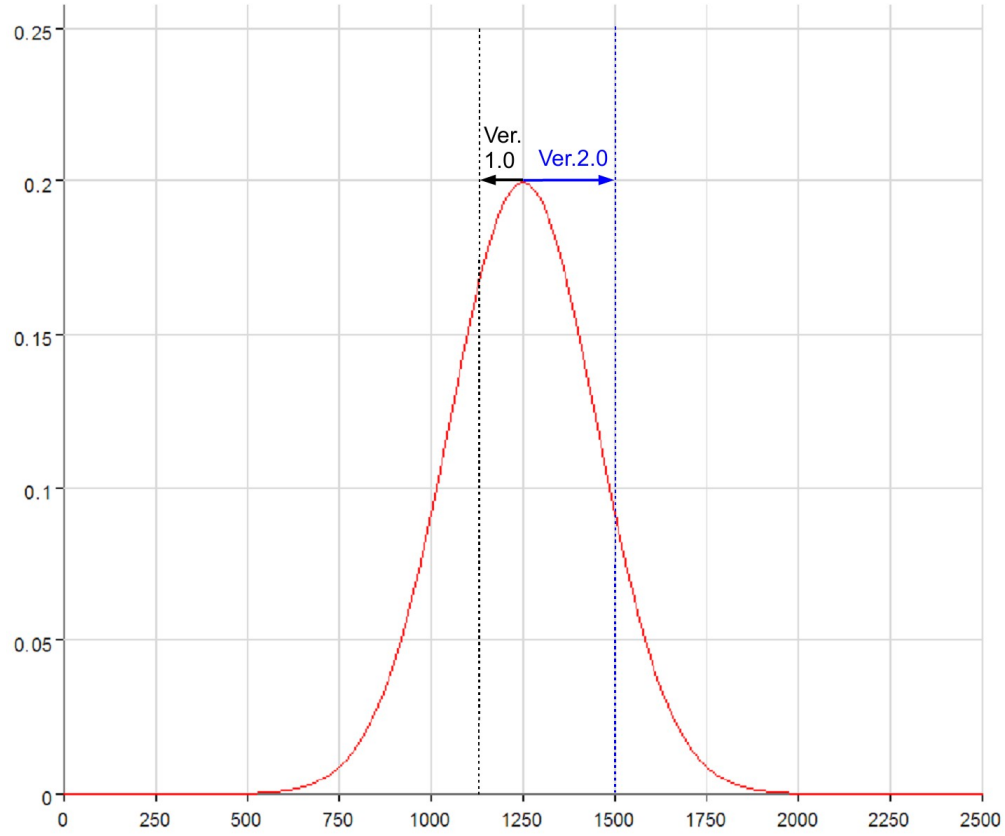

Figure 8. Halves of steps under change register TRIM value on minimal value in n-XYTER 1.0 and 2.0

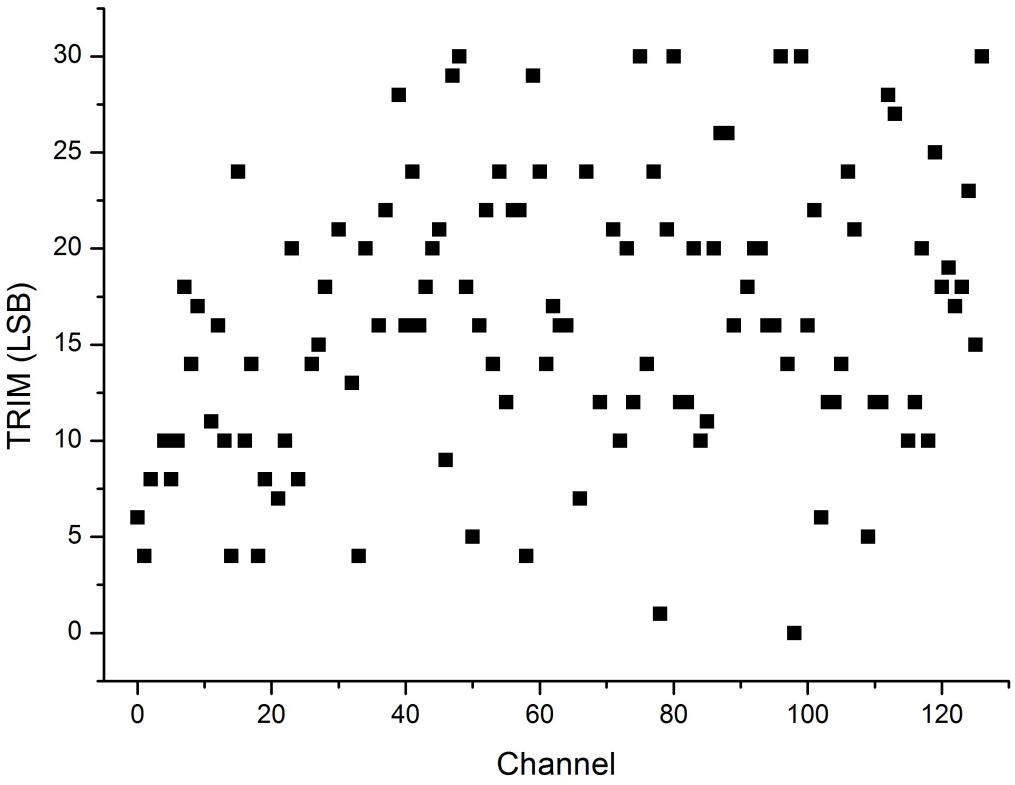

Figure 9. Register TRIM distribution.

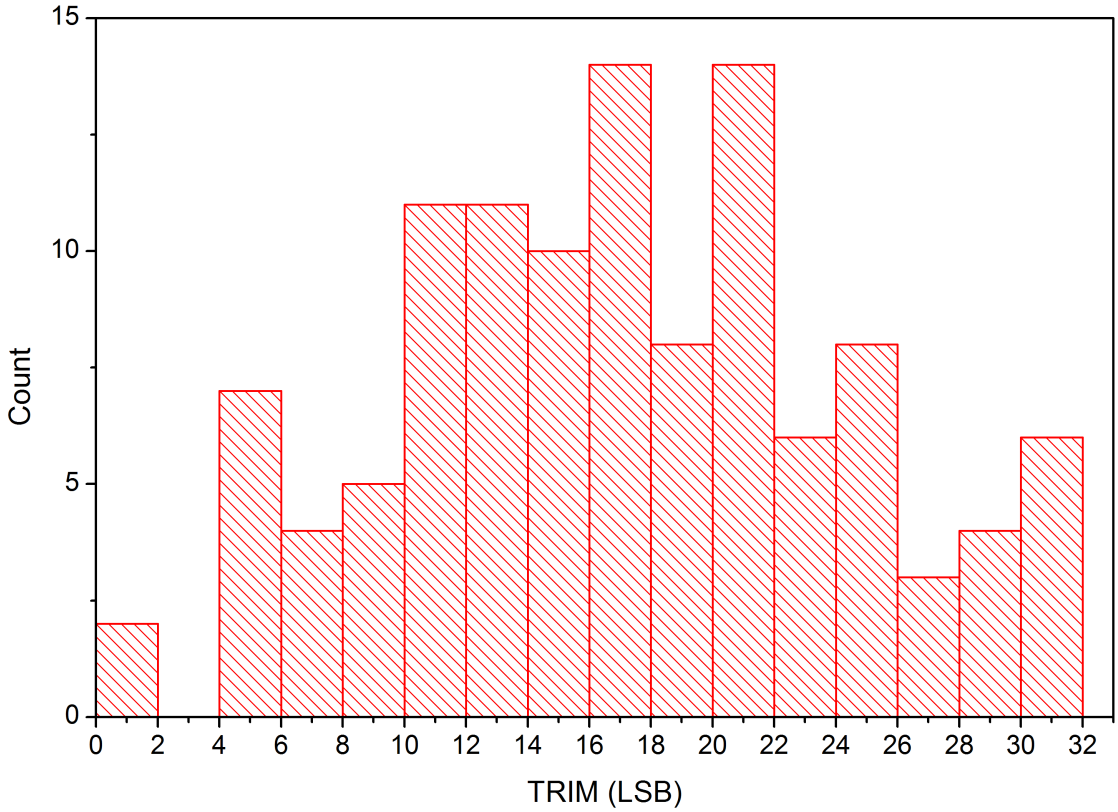

Figure 10. Histogram of register TRIM values.

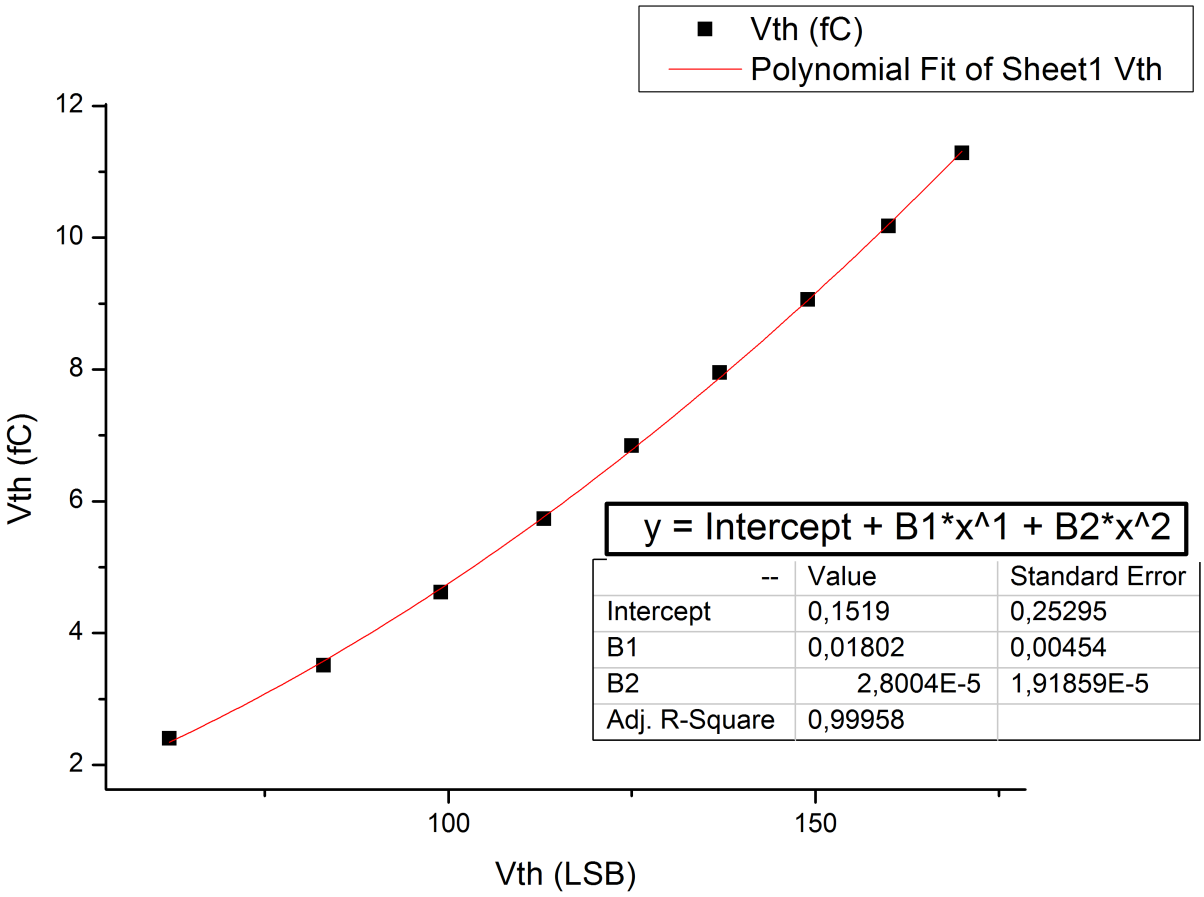

Figure 11. Calibration curve of value of *Vth* register.

6. Conclusion

In the process of Summer School script of fine adjustment of local threshold voltages in all channels of n-XYTER was created. This script was tested on two test benches, one of which was completely assembled by me. Algorithm was tested on n-XYTER ver. 1.0 and n-XYTER ver. 2.0. It is fully operational with n-XYTER ver. 1.0; during a testing with n-XYTER ver. 2.0 discreteness of TRIM register under changes of its in minimum value was 3 times bigger then its for n-XYTER ver. 1.0.

References

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