Testing and calibration of electronics for the BM@N ToF-400 system

Author:
Busin Svyatoslav
Russia National Research Nuclear UniversityMEPhI
Supervisors:
Vadim Babkin
Mikhail Rumyantsev
VyatcheslavGolovatyuk

Participation period
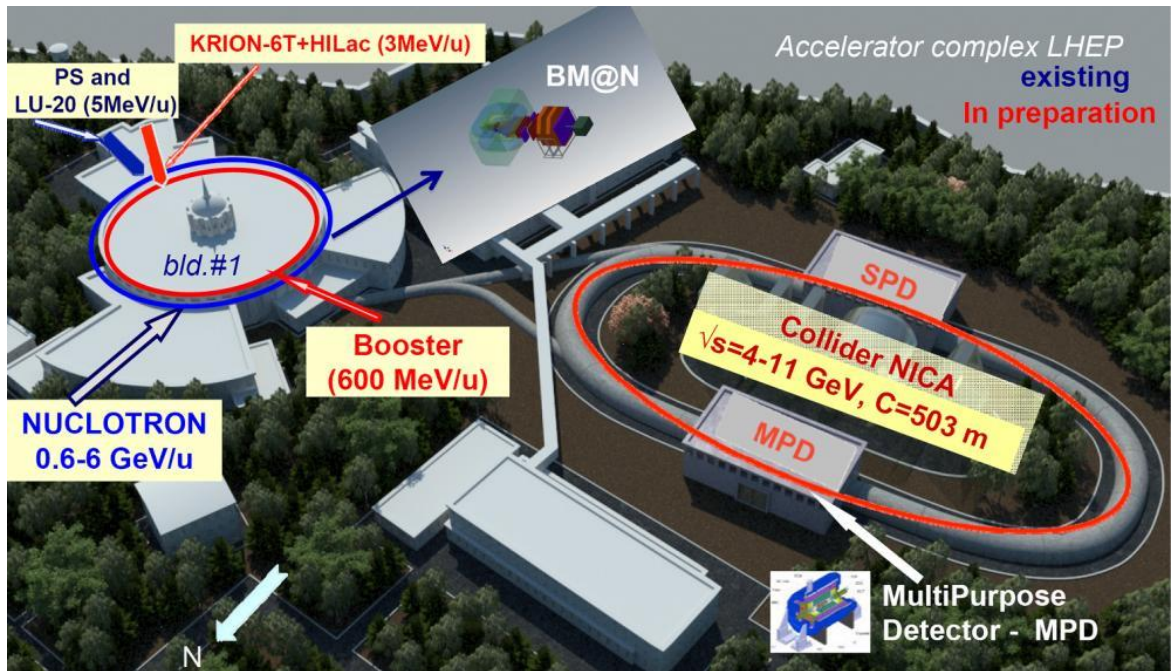9 July-26 August

Dubna2017

Contents

1. NICA project.

Fig. 1. Schematic view of the NICA-Nuclotron complex and the position of the BM@N setup.

The Nuclotron-based Ion Colider fAcility (NICA) is currently under construction at the Joint Institute for Nuclear Research [1]. The global aim of this project is to explore the phase diagram of strongly interacting matter in the region of highly compressed and hot baryonic matter. The BM@N is the first experiment of the NICA accelerator complex (Fig.1.) where extracted ion beams of the Nuclotron are used. The aim of the BM@N experiment is to study interactions of relativistic heavy ion beams (from *p* to *Au* with energy range of $1 - 6$ GeV/nucleon and the intensity of $\sim 10^{7}$ s^{-1}) with fixed targets. The detailed description of the BM@N experiment can be found in Ref. [2,3]
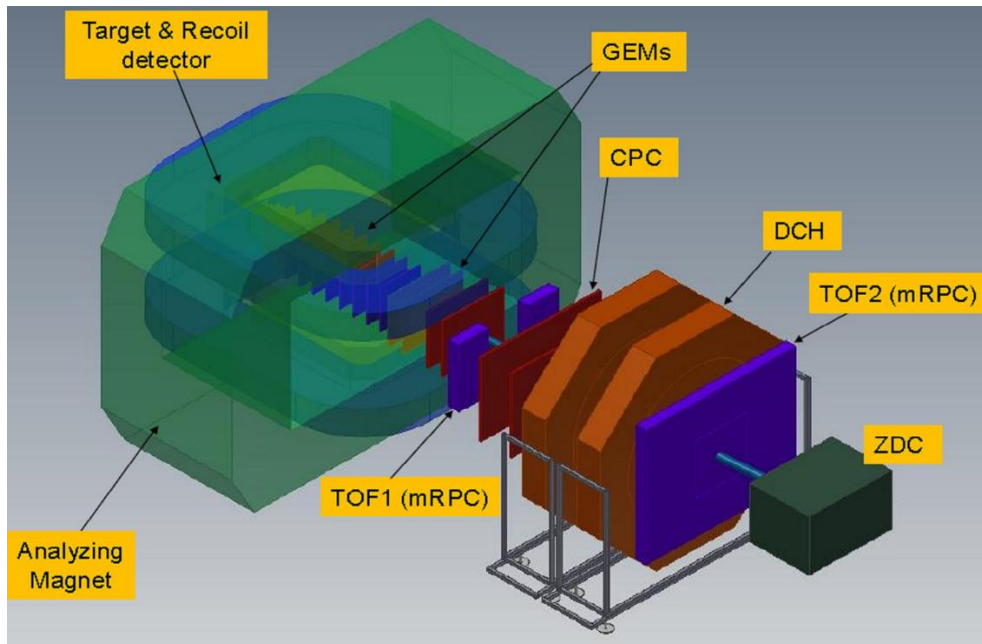
Fig. 2. Scheme of BM@N detector.

The general view of the BM@N detector is shown in Fig.2. The BM@N detector includes a large acceptance dipole magnet with the inner tracking system, which consists of double-side silicon-strip sensors and GEM detectors and has 12 layers. The outer tracker is based on the drift cambers (DCH) and cathode pad chambers (CPC). Particle identification in the experiment is performed using time-of-flight (ToF) system based on the mRPC technology. The ToF consists of two parts: low momentum (ToF-400 (1)) and high momentum (ToF-700 (2)). Zero-degree calorimeter (ZDC) is used for triggering and centrality determination. Electromagnetic calorimeter (ECal) is used for photons and leptons registration.

The aim of this work was assembling, testing and calibration of readout electronics for the BM@N ToF-400 system.

2.ToF-400 system

The ToF-400 system consists of two parts (left and right) that are placed symmetrical to a beam. Each part consists of two gas boxes each contents 5 mRPCs. The active area of the mRPCs overlap on 50 mm inside the box. Overlap of the gas boxes ensures crossing of the active area of detectors for 50 mm. The size of each part is 1.15x1.3 m^2 and defined to suffice the geometrical acceptance of the tracking detectors. Separation of pions/kaons up to 3 GeV/c requires time resolution better than 80 ps for the ToF-400 detectors.
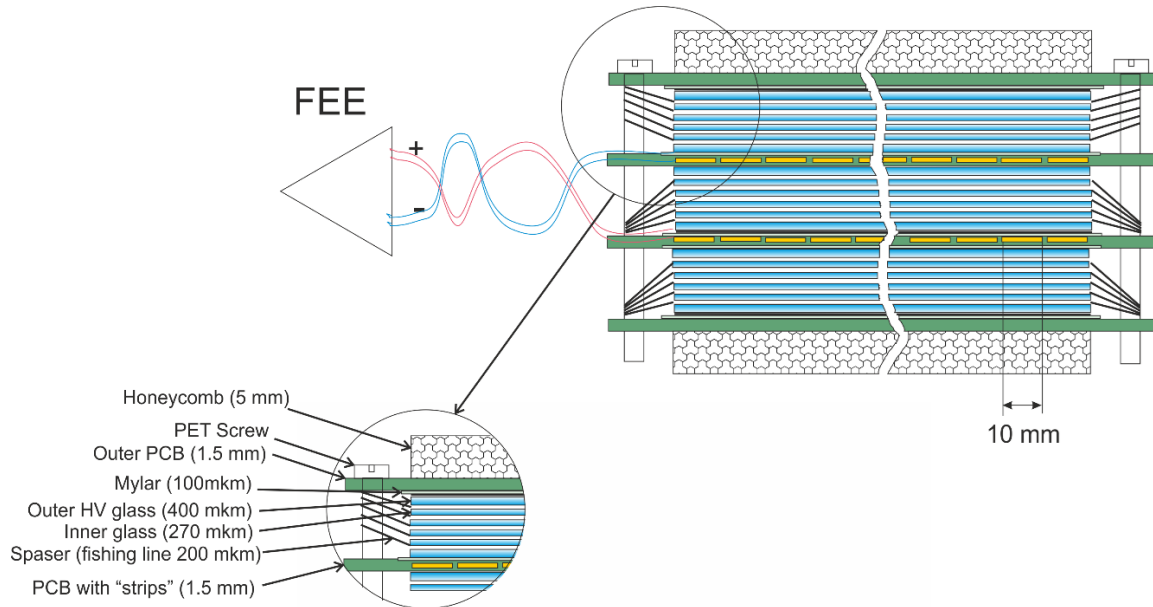
2.1 Mechanical construction of mRPC

Fig. 3. Sectional view of the triple stack strip mRPC for ToF-400.

The scheme of the mRPC is presented inFig. 3 [4]. The detector consists of three stacks of 5 gas gaps each. Common float glass is used as resistive electrodes. The outer glass electrodes have the thickness of 0.4 mm. The internal glass electrodes have the thickness of 0.27 mm. The fishing line as a spacer defines the 200 μm gap between all resistive electrodes. The outer part of external glass electrodes is covered by the conductive paint with the surface resistivity of about 2-10 MΩ/cm^2 to apply high voltage. All internal glasses are floating. The pickup electrodes look like strips and made at the printed circuit board (PCB). The main feature of the proposed triple-stack mRPC is that readout strips are located only in the inner stack. This ensures that the construction is symmetric, and the speed of signals on the anode and cathode are the same, which prevents the dispersion of the signal. For stiffening structure, the Kevlar honeycomb panels with the thickness of 10 mm were glued on the outer part of the external PCBs.

Dimension of the active area of one mRPC is 300*600 mm^2. It has 48 readout strips, 10 mm wide and 300 mm long. To reduce crosstalks, the gap between this strips is 2.5 mm. Thus the pitch of electrodes in this case is 12.5 mm.

Differential analog signal from a strip is transferred by twisted pair cable to front-end electronics. Signal is read out from both ends of the strip. It provides better time resolution and determination of the coordinate of a particle along strip.

2.2 Time-to-digital converter TDC72VHL

2-channel time-to-digital converters (TDC72VHL) based on the HPTDC chip [5] were developed and produced for digitization of LVDS signals and data acquisition (Fig. 4). First experiments on the mRPC time resolution evaluation in 2012 showed that large integral

nonlinearity (Fig. 5.) occurs with TDC that operats in the mode of 24.4 ps per bin. This nonlinearity causes strong degradation of time distribution. The contribution of this nonlinearity and the method to eliminate it has already been shown in the HPTDC Manual as well as in other publications.
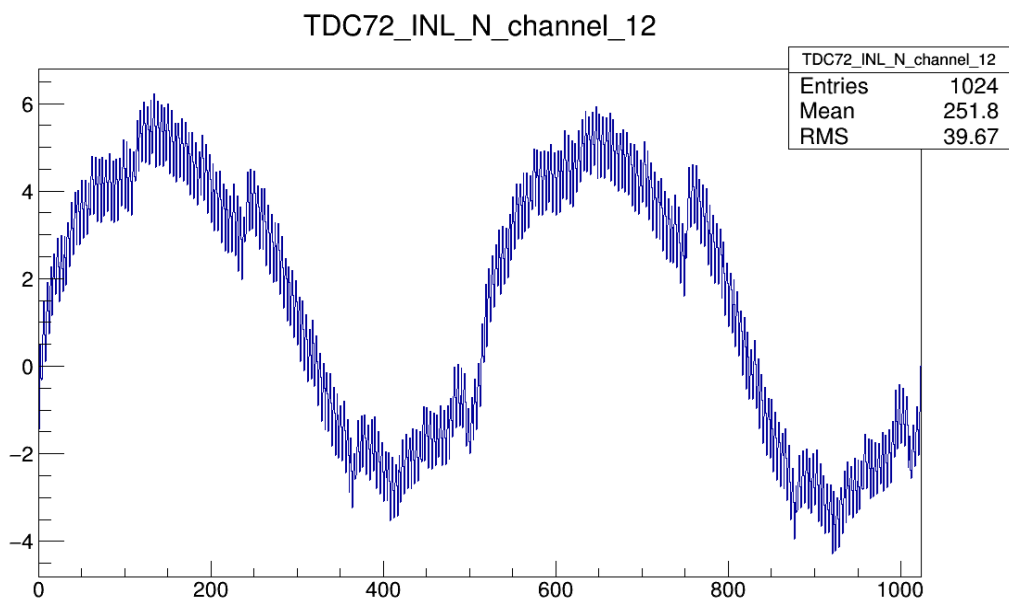

Fig. 4. View of the TDC72VHL module.

Fig. 5. Integral nonlinearity for one channel [bins].

3 Realization and methods

The method of uniform filling of a time gap with random events (code density test) was used for calibration (consideration of nonlinearity) of 16 VME TDC72VHL modules. A large statistics (~10 000 000 events per channel) was collected to minimize the statistical error (~1%). Signal from the photomultiplier was used as a trigger signal. The trigger reached U40VE (Universal 40 channel VME and Ethernet interface board) and the FVME2 trigger module through which information was exchanged with the client (Fig. 6.). The self-made LVDS generator (Fig.7.) was used for uniform filling of a time gap. Then the LVDS signal is transmitted to the TDC72VHL molex connector. Output data are written in a binary file (~8 Gb for one TDC). Then binary file with the data were decoded by BMNRoot for further processing.

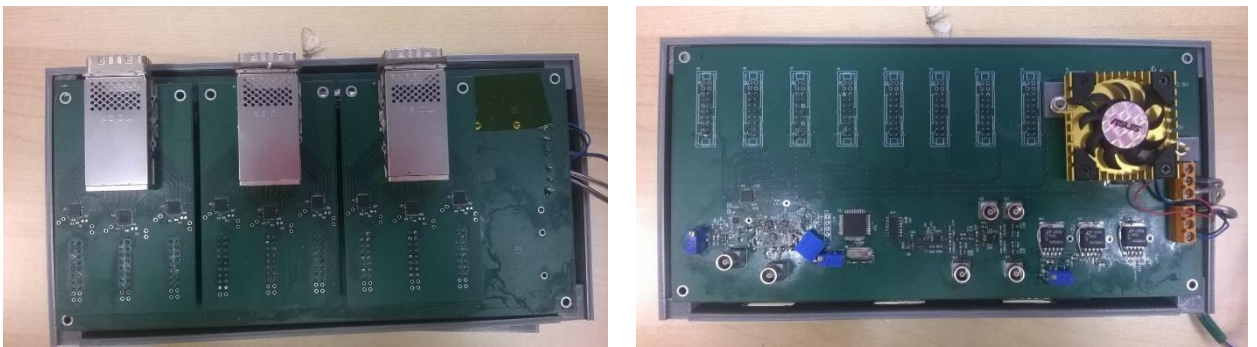Fig. 6. VME crate with U40VE, FVME2 and 16 TDC72VHL modules

Fig. 7. 72 channels LVDS generator

3.1 BmnRoot framework

The BM@N experiment uses a special software framework BmnRoot[6] to process and analyze the experimental data. This framework is built around the ROOT[7] environment and the FairSoft object-oriented framework FairRoot[8]. Overall, the BmnRoot is a powerful tool for BM@N detector performance studies, development of algorithms for reconstruction and physics analysis of the data. It also provides an interface for the PostgreSQL database, which will be used in this work to download the necessary data. The BmnRoot framework is written in C++.

To perform a decoding process from the raw binary experimental data to a ROOT TTree file, the class BmnRawDataDecoder is included in the frame-work. The TDC information after the first stage is stored in a BmnTDCDigit class. The BmnTDCDigit class stores only one TDC digit (TDC measurement) and has the following fields inside:

- Crate serial and slot, in which the current VHL module is inserted;
- VHL module type (0x12 for the TDC72VHL TDC);
- HPTDC chip's id;
- HPTDC chip channel index;
- Type of the TDC digit: leading or trailing;
- Time (value) of the digit in the TDC bins.

The BmnRawDataDecoder class uses the BmnTof1Raw2Digit::FillEvent method to convert an array of the BmnTDCDigit structures into Tof-400 data. The Tof-400 data are stored in the BmnTof1Digit structure. The BmnTof1Digit structure stores the plane id, strip index, side of the strip, leading time of the signal and its width.

3.2 INL Correction

As it is said above, the usage of the 24 ns mode, in which the HPTDC chips operate in the TDC72VHL module, leads to a large nonlinearity. To overcome this problem, this nonlinearity should be measured and then corrected using these collected data. To define the INL (integral nonlinearity), term the DNL (differential non- linearity) must be defined. The DNL for each of 1024 bins can be calculated using the equation:

$$DNL = \frac{W^R - W^t}{W^t}$$

Here W^R is the real bin time width and $W^t = 24$ $ns/1024$ is a perfect bin width. One can measure the DNL for each bin of each channel in the TDC72VHL module by applying a uniform-distributed in time LVDS pulse signals to the input of the TDC72VHL and calculating the number of events in each bin. Hypothetically, the number of events in each bin should be proportional to the bin width, and, if the HPTDC chips were perfect (without any nonlinearity),

number of the events in each bin would be the same. In fact, the number of events varies from bin to bin, so does the bin width. Using such a procedure, one can find each bin's real width and, therefore, the differential nonlinearity. The integral nonlinearity is defined as a sum over all of the DNL in "previous" bins:

$$INL_i = \sum_{j=0}^{i} DNL_j$$

To convert the TDC Digit value v to real time in *ns* with the appliance of the nonlinearity correction, one can use the following equation

$$t = \sum_{i=0}^{v\%1024} W_i^R + \frac{v}{1024} \times 24.4 = \sum_{i=0}^{v\%1024} DNL \times W^t + W^t \times (v\%1024) + \frac{v}{1024} \times 24.4,$$

where x%y is the remainder of x divided by y.

In terms of INL characteristics, this equation can be simplified in the following formula:

$$t = (v + INL_{v\%1024}) \times \frac{24}{1024} ns$$

Due to the comparative simplicity of this formula, INL characteristics are used to store the nonlinearity data and to apply the correction. The example INL characteristics for one channel are given in Fig. 5. The INL characteristics are stored in the text file for each channel and the TDC module separately as an array of bin number and INL value. The size of this array is equal to the number of bins – 1024.

3.3 Check INL correction

To check INL corrections was used delay between leading and trailing. One channel was used as fixed channel the other one was delayed. The Stanford Digital Delay Generator DG645 was used to provide delay between two channels (Fig. 8). The DG645 is a versatile digital delay/pulse generator that provides precisely defined pulses at the repetition rates up to 10 MHz. The instrument offers several improvements over older designs — lower jitter, higher accuracy, faster trigger rates, and more outputs. The DG645 also has Ethernet, GPIB and RS-232 interfaces for computer or network control of the instrument [9]. DG645 can be easily controlled from PC that allows to automating the data set.

Time difference between a fix channel and a delayed channel was chosen as the criteria of INL correction. Fig.9 shows the time difference with the delay from 0 to 13 ns with the step of 0.5 ns without the INL correction.
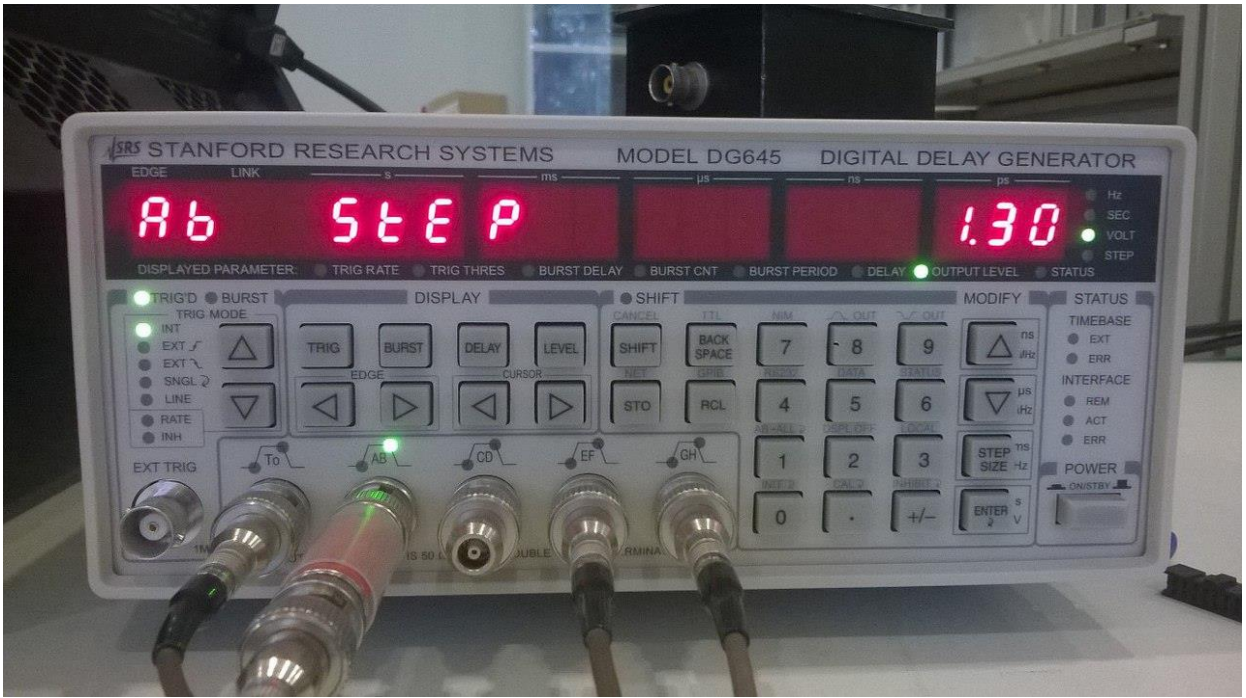
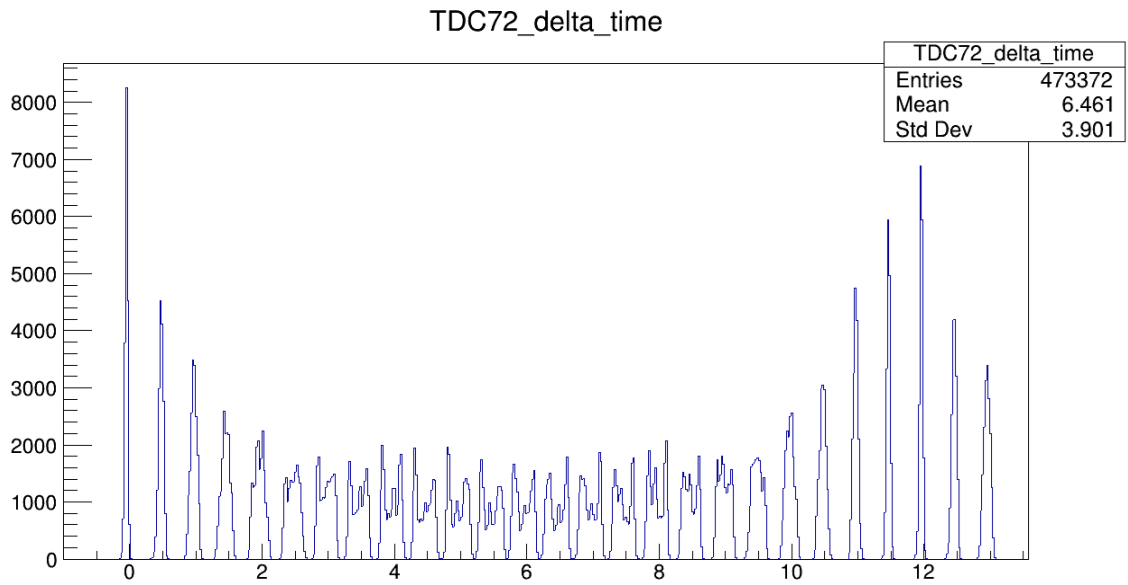Fig. 8. SRS Digital Delay Generator DG645

Fig. 9. Time difference between fixed and delayed channel [ns].

In this figure, you can see bad time resolution in the central area due to the high integral nonlinearity.
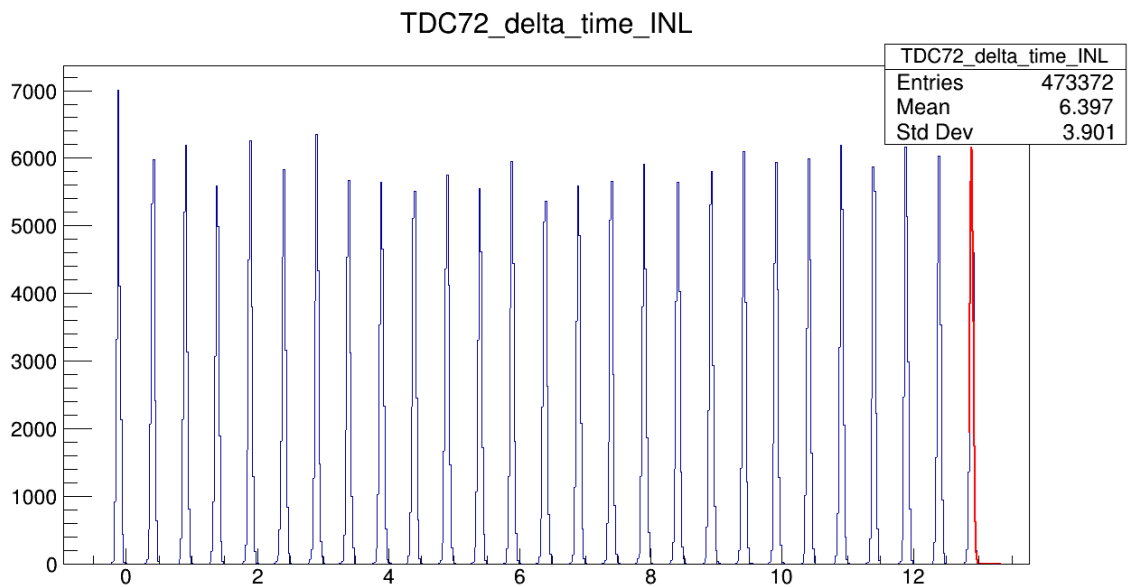
Fig. 10. Time difference between fix and delayed channels with INL corrections.

After applying the INL calibration, the time resolution between two channels became much better.

Conclusion

INL calibration was tested and performed for 16 TDC72 for each channel. During the experiment, jitter of electronics (~32 ps) was detected. Because that, time resolution between two channels does not exceed 40 ps. The conducted experiment showed consistency of the INL correction. Before data setting, it is necessary to measure jitter and take it into account when processing data.

References

[1] http://nica.jinr.ru/

[2] Conceptual Design Report. Study of Strange Matter Production in Heavy-Ion Collisions at the Nuclotron. 170pp.http://nica.jinr.ru/files/BM@N/BMN_CDR.pdf

[3] BM@N proposal for JINR-PAC Meeting. Study of Strange MatterProduction in the Heavy Ion Collisions at Nuclotron. January 10, 2012.28pp.http://nica.jinr.ru/files/BM@N/BMN_Project_JINR_PAC_Jan2012.pdf

[4] V. Babkin, et al., *Triple-stack multigap resistive plate chamber with strip readout*, Nucl. Instrum Meth.(2015), http://dx.doi.org/10.1016/j.nima.2015.11.060

[5] J. Christiansen. *High performance time to digital converter (HPTDC)*, Digital Microelec. Group, CERN, HPTDC manual version 2.2 for HPTDC version 1.3.

[6] NICA / Bmnroot − Simulation and Analysis Framework for NICA/BM@NDetectors. https://git.jinr.ru/nica/bmnroot

[7] Root - Cern. An object oriented framework for large scale data analysis.https://root.cern.ch/

[8] FairRoot. https://fairroot.gsi.de/

[9] DG645 User Manual Stanford Research Systems